AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (previously presented) A method of simulating the operation of a data processing apparatus to determine timing information of data transfers, the data processing apparatus comprising a number of master logic units and slave logic units coupled via a bus, the data processing apparatus being operable to perform the data transfers between the master logic units and the slave logic units over the bus, the method comprising the steps of:

a) generating anticipated timing information for each successive data transfer over the bus by assuming that each successive data transfer can occur with exclusive access to the bus;

b) determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus; and

c) in the event that the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus, generating machine-readable revised timing information for those data transfers for use in correcting said anticipated timing information as part of simulation output results, the revised timing information being generated using bus status information until those data transfers have been completed.

2. (original) The method as claimed in claim 1, wherein the step a) further comprises the step of generating anticipated timing information for each successive data transfer between one master logic unit and one slave logic unit over the bus to which that master logic unit and that slave logic unit have exclusive access.

3. (original) The method as claimed in claim 1, wherein the anticipated timing information comprises a data transfer window indicative of the time during which that data transfer will occur over the bus.

4. (original) The method as claimed in claim 1, wherein the anticipated timing information comprises data transfer commencement information indicative of the time at which that data transfer will commence on the bus and data transfer completion information indicative of the time at which that data transfer will complete on the bus.

5. (original) The method as claimed in claim 1, wherein each data transfer comprises the transfer of a number of data values over the bus and the anticipated timing information comprises data value transfer information indicative of the time at which each data value will be transferred over the bus.

6. (original) The method as claimed in claim 1, wherein the step b) further comprises the step of comparing the anticipated timing information for each successive data transfer to determine whether two or more concurrent data transfers would occur on the bus.

7. (original) The method as claimed in claim 6, wherein the step b) further comprises the step of determining whether two or more concurrent data transfers would occur on the bus by determining whether the anticipated timing information indicates that one data transfer will not complete prior to another data transfer commencing.

8. (original) The method as claimed in claim 1, wherein the step c) further comprises the step of generating bus status information indicative of the status of the bus during at least a period when the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus.

9. (original) The method as claimed in claim 8, wherein the bus status information includes information indicative of which master logic unit/slave logic unit pair have access to the bus at any point in time during at least the period.

10. (original) The method as claimed in claim 8, wherein the step c) further comprises the step determining from the generating bus status information which of those data transfers will occur on the bus at any point in time during at least the period.

11. (original) The method as claimed in claim 9, wherein the step c) further comprises the step of generating revised timing information indicative of the time during which each of those data transfers occur over the bus.

12. (previously presented) A method of simulating the operation of a data processing apparatus using a software model to determine timing information of data transfers, the data processing apparatus comprising a number of master logic units and slave logic units coupled via a bus, the data processing apparatus being operable to perform the data transfers between the master logic units and the slave logic units over the bus, the method comprising the steps of:

a) in response to an indication that a data transfer is to occur, generating data transfer information indicative of the data transfer using a master logic unit model and a slave logic unit model;

b) generating anticipated timing information from the data transfer information using the master logic unit model and the slave logic unit model, the anticipated timing information being generated by assuming that the data transfer will occur with exclusive access to the bus;

c) determining from the anticipated timing information whether two or more concurrent data transfers will occur on the bus; and

d) in the event that is it anticipated that two or more concurrent data transfers will occur on the bus, generating machine-readable revised timing information for those data transfers using the master logic unit model and the slave logic unit model, the revised timing information being generated by modelling the status of the bus during at least the period when it is anticipated that two or more concurrent data transfers will occur.

13. (original) The method as claimed in claim 12, wherein the data transfer information includes information indicative of the type and size of data transfer.

14. (original) The method as claimed in claim 12, wherein the step b) comprises generating anticipated timing information comprising timing values generated by the master logic unit model and the slave logic unit model indicative of the time during which that data transfer will occur over the bus.

15. (original) The method as claimed in claim 12, wherein the step b) comprises gencrating anticipated timing information comprising data transfer commencement information using the master logic unit model, the data transfer commencement information being indicative of the time at which that data transfer will commence on the bus and generating data transfer completion information using the slave logic unit model, the data transfer completion information being indicative of the time at which that data transfer will complete on the bus.

16. (original) The method as claimed in claim 12, wherein each data transfer comprises the transfer of a number of data values over the bus and the step b) comprises generating anticipated timing information comprising data value transfer information indicative of the time at which each data value will be transferred over the bus.

17. (original) The method as claimed in claim 12, wherein the step c) further comprises the step of comparing the anticipated timing information for each successive data transfer using a arbiter model to determine whether two or more concurrent data transfers would occur on the bus.

18. (original) The method as claimed in claim 17, wherein the step c) further comprises the step of determining whether two or more concurrent data transfers would occur on the bus by determining whether the anticipated timing information indicates that one data transfer will not complete prior to another data transfer commencing.

19. (original) The method as claimed in claim 12, further comprising the step of:

generating a transaction including the data transfer information.

20. (original) The method as claimed in claim 19, wherein the steps a) and b) comprise the steps of:

generating master data transfer information and master anticipated timing information from the data transfer information using a master logic unit model;

storing the master data transfer information and the master anticipated timing information in the transaction;

passing the transaction to the slave logic unit model;

generating slave data transfer information and slave anticipated timing information from the data transfer information using a slave logic unit model; and

storing the slave data transfer information and the slave anticipated timing information in the transaction.

21. (original) The method as claimed in claim 19, wherein the step c) further comprises the steps of:

passing the transaction to an arbiter model;

updating a bus allocation table with the anticipated timing information in the transaction;

determining from the bus allocation table whether two or more concurrent data transfers are anticipated to occur.

22. (original) The method as claimed in claim 19, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of:

causing each master logic unit model and slave logic unit model associated with the two or more concurrent data transfers to initialise timing models operable to simulate bus signals generated by each of the corresponding master logic units and slave logic units on a clock cycle by clock cycle basis.

23. (original) The method as claimed in claim 22, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the steps of:

setting a current clock cycle from which the bus signals are to be simulated;

initialising the timing models based on the current clock cycle and using anticipated timing information within the transactions associated with the two or more concurrent data transfers.

24. (original) The method as claimed in claim 22, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of:

determining, using an arbiter model and based on the simulated bus signals, which of the master logic unit models and slave logic unit models will be allocated access to the bus during any particular clock cycle.

25. (original) The method as claimed in claim 24, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of:

signalling the master logic unit models and slave logic unit models with the outcome of the determination.

26. (original) The method as claimed in claim 25, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of:

on receipt of a signal indicating to a master logic unit model or slave logic unit model that access to the bus has been granted, generating the revised timing information indicative of the actual clock cycles over which the data transfer occurred.

27. (original) The method as claimed in claim 22, wherein once the revised timing information has been generated for two or more concurrent data transfers, simulating bus signals generated by each of the corresponding master logic units and slave logic units on a clock cycle by clock cycle basis is suspended.

28. (original) The method as claimed in claim 12, wherein in the event that is it anticipated that two or more concurrent data transfers will not occur, the step d) further comprises the step of:

causing the associated master logic unit model and slave logic unit model to remain inactive for the period of the data transfer.

29. (previously presented) Apparatus for simulating the operation of a data processing apparatus to determine timing information of data transfers, the data processing apparatus comprising a number of master logic units and slave logic units coupled via a bus, the data processing apparatus being operable to perform the data transfers between the master logic units and the slave logic units over the bus, the apparatus comprising a computer for executing a plurality of software models including:

a master logic unit software model and a slave logic unit software model each being operable, in response an indication that a data transfer is to occur, to generate data transfer information indicative of the data transfer, the master logic unit software model and the slave logic unit software model being further operable:

in a default mode to generate anticipated timing information from the data transfer information, the anticipated timing information being generated by assuming that the data transfer will occur with exclusive access to the bus, and

in a selected mode, when it is anticipated that two or more concurrent data transfers will occur on the bus, to generate computer-readable revised timing information for those data transfers for use in correcting said anticipated timing information as part of simulation output results, the revised timing information being generated by modelling the status of the bus during at least the period when it is anticipated that the two or more concurrent data transfers will occur; and

a bus software model operable to determine from the anticipated timing information whether two or more concurrent data transfers will occur and, when it is anticipated that two or

more concurrent data transfers will occur, to signal the master logic unit software model and the slave logic unit software model to switch from the default mode to the selected mode.

30. (previously presented) The apparatus as claimed in claim 29, wherein the data transfer information includes information indicative of the type and size of data transfer.

31. (previously presented) The apparatus as claimed in claim 29, wherein the master logic unit software model and the slave logic unit software model are operable to generate anticipated timing information comprising timing values indicative of the time during which that data transfer will occur over the bus.

32. (previously presented) The apparatus as claimed in claim 29, wherein the master logic unit software model is operable to generate anticipated timing information comprising data transfer commencement information, the data transfer commencement information being indicative of the time at which that data transfer will commence on the bus and the slave logic unit software model is operable to generate anticipated timing information comprising data transfer completion information, the data transfer completion information being indicative of the time at which that data transfer will complete on the bus.

33. (previously presented) The apparatus as claimed in claim 29, wherein each data transfer comprises the transfer of a number of data values over the bus and the master logic unit software model and the slave logic unit software model are operable to generate anticipated

timing information comprising data value transfer information indicative of the time at which each data value will be transferred over the bus.

34. (previously presented) The apparatus as claimed in claim 29, wherein the arbiter model is operable to compare the anticipated timing information for each successive data transfer to determine whether two or more concurrent data transfers would occur on the bus.

35. (previously presented) The apparatus as claimed in claim 34, wherein the arbiter model is operable to determine whether two or more concurrent data transfers would occur on the bus by determining whether the anticipated timing information indicates that one data transfer will not complete prior to another data transfer commencing.

36. (previously presented) The apparatus as claimed in claim 29, wherein the master logic unit software model and the slave logic unit software model are operable to generate a transaction including the data transfer information.

37. (previously presented) The apparatus as claimed in claim 36, wherein the master logic unit model is operable to generate master data transfer information and master anticipated timing information from the data transfer information and to store the master data transfer information and the master anticipated timing information in the transaction and the slave logic unit model is operable to generate slave data transfer information and slave anticipated timing information from the data transfer information and to store the slave data transfer information and the slave anticipated timing information in the transaction.

38. (previously presented) The apparatus as claimed in claim 37, wherein the arbiter model is operable to update a bus allocation table with the anticipated timing information in the transaction and to determine from the bus allocation table whether two or more concurrent data transfers are anticipated to occur.

39. (previously presented) The apparatus as claimed in claim 36, wherein in the event that is it anticipated that two or more concurrent data transfers will occur, each master logic unit model and slave logic unit model associated with the two or more concurrent data transfers are operable to initialise timing models operable to simulate bus signals generated by each of the corresponding master logic units and slave logic units on a clock cycle by clock cycle basis.

40. (previously presented) The apparatus as claimed in claim 39, wherein in the event that is it anticipated that two or more concurrent data transfers will occur each master logic unit model and slave logic unit model associated with the two or more concurrent data transfers are operable to set a current clock cycle from which the bus signals are to be simulated, to initialise the timing models based on the current clock cycle and to use anticipated timing information within the transactions associated with the two or more concurrent data transfers.

41. (previously presented) The apparatus as claimed in claim 39, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the arbiter model is operable to determine, based on the simulated bus signals, which of the master logic unit models and slave logic unit models will be allocated access to the bus during any particular clock cycle.

42. (previously presented) The apparatus as claimed in claim 41, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the arbiter model is operable to signal the master logic unit models and slave logic unit models with the outcome of the determination.

43. (previously presented) The apparatus as claimed in claim 42, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the master logic unit model or slave logic unit model receiving a signal indicating that access to the bus has been granted is operable to generate the revised timing information indicative of the actual clock cycles over which the data transfer occurred.

44. (previously presented) The apparatus as claimed in claim 39, wherein once the revised timing information has been generated for two or more concurrent data transfers the operation of the timing models is suspended.

45. (previously presented) The apparatus as claimed in claim 29, wherein in the event that is it anticipated that two or more concurrent data transfers will not occur, the associated master logic unit model and slave logic unit model are instructed to remain inactive for the period of the data transfer.

46. (currently amended) A computer program storage medium storing a computer program ~~for simulation~~ for simulating the operation of a data processing apparatus to determine

timing information of data transfers, the data processing apparatus comprising a number of master logic units and slave logic units coupled via a bus, the data processing apparatus being operable to perform the data transfers between the master logic units and the slave logic units over the bus, the computer program comprising:

a master logic unit software model and a slave logic unit software model each being operable, in response an indication that a data transfer is to occur, to generate data transfer information indicative of the data transfer, the master logic unit software model and the slave logic unit software model being further operable

in a default mode to generate anticipated timing information from the data transfer information, the anticipated timing information being generated by assuming that the data transfer will occur with exclusive access to the bus and

in a selected mode, when it is anticipated that two or more concurrent data transfers will occur on the bus, to generate machine-readable revised timing information for those data transfers for use in correcting said anticipated timing information as part of simulation output results, the revised timing information being generated by modelling the status of the bus during at least the period when it is anticipated that the two or more concurrent data transfers will occur; and

a bus software model operable to determine from the anticipated timing information whether two or more concurrent data transfers will occur and, when it is anticipated that two or more concurrent data transfers will occur, to signal the master logic unit software model and the slave logic unit software model to switch from the default mode to the selected mode.